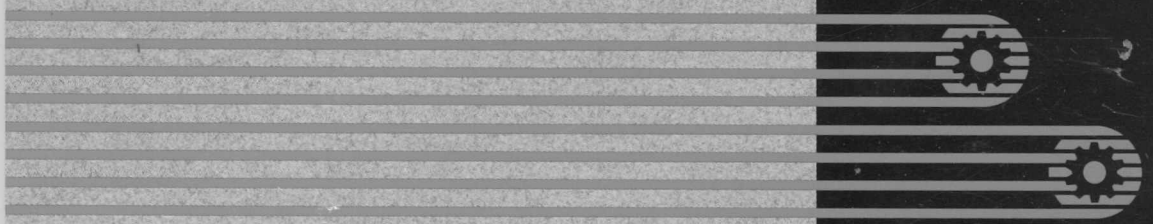
8XC196MD Manual Supplement
8XC196MC Manual Errata



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SECTION I

Overview of New MD Features

1

Overview of New MD Features

CHAPTER 1
OVERVIEW OF NEW MD FEATURES

The 8XC196MD is the newest member of the MCS-96 motor control family. The 8XC196MD includes all of the 8XC196MC features, and adds the following enhancements:

A frequency generator allows generating a programmable frequency square wave, which finds use in infrared remote control communications.

Two additional capture/compare and two compare only modules are added to the Event Processor Array, giving additional event capture and generation capabilities.

Eight additional I/O pins, two digital input only pins, and one analog/digital input pin are added.

The 8XC196MD maintains pin-for-pin compatibility with the 8XC196MC device, allowing easy upgrades of existing designs.

Figure 1.1 illustrates the block diagram for the 8XC196MD:

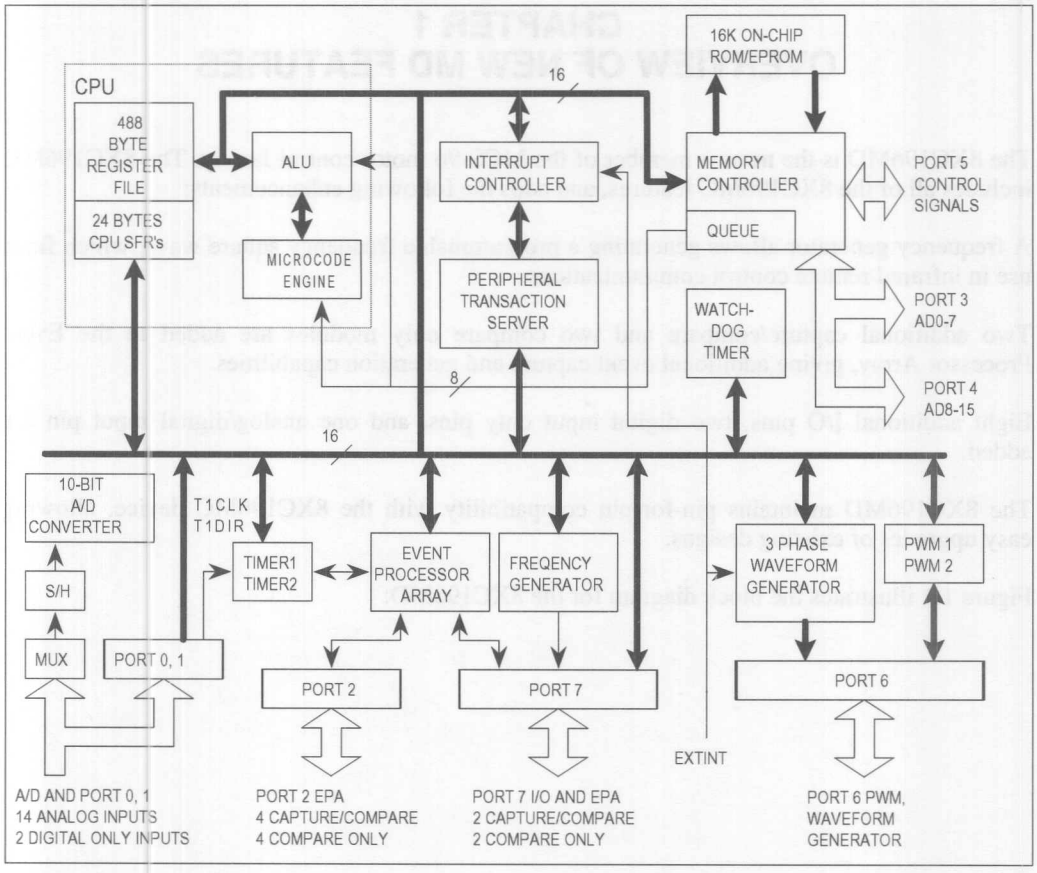

Figure 1.1. 8XC197MD Block Diagram

Pinout Differences 2

Pinout Differences

CHAPTER 2
PINOUT DIFFERENCES:

The 8XC196MD is designed to be plug-in compatible with the 8XC196MC device. Eleven new pin functions have been added to the MD, increasing I/O capabilities and providing additional peripheral features.

Most of the additional pins on the MD were N.C. (no connects) on the MC device. However, P1.6 and P1.7 on the MD are digital inputs, while on the MC this is connected to Vss and N.C. respectively. Also, P1.5 on the MD is an analog input, while on the MC this is connected to Vss. If these pins are not needed by an application, they should remain connected to Vss.

The 8XC196MD is available in the 84-lead PLCC and 80-lead QFP packages. Tables 2.1 and 2.2 document the pin names for the 8XC196MC and 8XC196MD devices:

Table 2.1. 8XC196MD 84-lead PLCC Package Pinout

PLCC Pin #	Description
1	P5.4
2	P5.6/READY
3	P5.1/INST
4	Vss
5	P5.0/ALE
6	Vpp
7	P5.3/$\overline{RD}$
8	P5.5/$\overline{BHE}$
9	N.C.
10	P5.2/$\overline{WR}$/$\overline{WRL}$
11	P5.7/BUSWIDTH
12	P4.7/AD15
13	P4.6/AD14
14	Vcc
15	P4.5/AD13
16	CLKOUT
17	P4.4/AD12
18	P4.3/AD11
19	P4.2/AD10
20	P4.1/AD09
21	P4.0/AD08
22	N.C.
23	N.C.
24	P3.7/AD07
25	P3.6/AD06
26	P3.5/AD05
27	P3.4/AD04
28	P3.3/AD03
29	P3.2/AD02
30	P3.1/AD01
31	P3.0/AD00
32	**P1.7* (NC)**
33	$\overline{RESET}$
34	NMI
35	N.C.
36	$\overline{EA}$
37	**P1.6* (Vss)**
38	Vss
39	Vcc
40	P6.5/WG3
41	P6.4/$\overline{WG3}$
42	P6.3/WG2

PLCC Pin #	Description
43	Vss
44	P6.2/$\overline{WG2}$
45	P6.1/WG1
46	P6.0/$\overline{WG1}$
47	P1.3/ACH11/T1DIR
48	P1.2/ACH10/T1CLK
49	**P1.5/ACH13* (Vss)**
50	P1.4/ACH12
51	P1.1/ACH9
52	P1.0/ACH8
53	P0.7/ACH7/PMODE.3
54	P0.6/ACH6/PMODE.2
55	AGND
56	Vref
57	P0.5/ACH5/PMODE.1
58	P0.4/ACH4/PMODE.0
59	P0.3/ACH3
60	P0.2/ACH2
61	P0.1/ACH1
62	P0.0/ACH0
63	**P7.7/FREQOUT* (NC)**
64	P2.0/CAPCOMP0/$\overline{PVER}$
65	P2.1/CAPCOMP1/$\overline{PALE}$
66	**P7.0/CAPCOMP4* (NC)**
67	**P7.1/CAPCOMP5* (NC)**
68	P2.2/CAPCOMP2/PROG
69	P2.3/CAPCOMP3
70	P2.7/COMPARE3
71	**P7.2/COMPARE4* (NC)**
72	**P7.3/COMPARE5* (NC)**
73	P2.4/COMPARE0/$\overline{AINC}$
74	P2.5/COMPARE1/$\overline{PACT}$
75	P2.6/COMPARE2/CPVER
76	P6.7/PWM1
77	P6.6/PWM0
78	**P7.4* (NC)**
79	**P7.5* (NC)**
80	**P7.6* (NC)**
81	XTAL2
82	XTAL1
83	Vss
84	EXTINT

*** = New pin on 8XC196MD ( ) = 8XC196MC Function**

Table 2.2. 8XC196MD 80-lead QFP Package Pinout

QFP Pin #	Description
1	P5.2/$\overline{WR}$/$\overline{WRL}$
2	P5.7/BUSWIDTH
3	P4.7/AD15
4	P4.6/AD14
5	Vcc
6	P4.5/AD13
7	CLKOUT
8	P4.4/AD12
9	P4.3/AD11
10	P4.2/AD10
11	P4.1/AD09
12	P4.0/AD08
13	P3.7/AD07
14	P3.6/AD06
15	P3.5/AD05
16	P3.4/AD04
17	P3.3/AD03
18	P3.2/AD02
19	P3.1/AD01
20	P3.0/AD00
21	**P1.7* (NC)**
22	$\overline{RESET}$
23	NMI
24	$\overline{EA}$
25	Vss
26	**P1.6* (Vss)**
27	Vcc
28	P6.5/WG3
29	P6.4/$\overline{WG3}$
30	P6.3/WG2
31	Vss
32	P6.2/$\overline{WG2}$
33	P6.1/WG1
34	P6.0/$\overline{WG1}$
35	P1.3/ACH11/T1DIR
36	P1.2/ACH10/T1CLK
37	**P1.5/ACH13* (Vss)**
38	P1.4/ACH12
39	P1.1/ACH9
40	P1.0/ACH8

QFP Pin #	Description
41	P0.7/ACH7/PMODE.3
42	P0.6/ACH6/PMODE.2
43	AGND
44	Vref
45	P0.5/ACH5/PMODE.1
46	P0.4/ACH4/PMODE.0
47	P0.3/ACH3
48	P0.2/ACH2
49	P0.1/ACH1
50	P0.0/ACH0
51	**P7.7/FREQOUT* (NC)**
52	P2.0/CAPCOMP0/$\overline{PVER}$
53	P2.1/CAPCOMP1/$\overline{PALE}$
54	**P7.0/CAPCOMP4* (NC)**
55	**P7.1/CAPCOMP5* (NC)**
56	P2.2/CAPCOMP2/PROG
57	P2.3/CAPCOMP3
58	P2.7/COMPARE3
59	**P7.2/COMPARE4* (NC)**
60	**P7.3/COMPARE5* (NC)**
61	P2.4/COMPARE0/$\overline{AINC}$
62	P2.5/COMPARE1/$\overline{PACT}$
63	P2.6/COMPARE2/CPVER
64	P6.7/PWM1
65	P6.6/PWM0
66	**P7.4* (NC)**
67	**P7.5* (NC)**
68	**P7.6* (NC)**
69	XTAL2
70	XTAL1
71	Vss
72	EXTINT
73	P5.4
74	P5.6/READY
75	P5.1/INST
76	Vss
77	P5.0/ALE
78	Vpp
79	P5.3/$\overline{RD}$
80	P5.5/$\overline{BHE}$

*** = New pin on 8XC196MD ( ) = 8XC196MC Function**

Additional Port 1 Channels

3

Additional Port 1 Channels

CHAPTER 3
ADDITIONAL PORT 1 CHANNELS

Three additional channels have been added to Input port 1. P1.5 is an additional analog or digital input channel. P1.5 is assigned to analog channel 13, and is accessed by writing the value xDH to the AD_COMMAND register (where x represents the command). The digital value of pin P1.5 is read from the P1_PIN.5 register bit at location 1FA9H (Figure 1.1).

P1.6 and P1.7 are digital input only channels. These channels are accessed by reading P1_PIN.6 and PI_PIN.7 register bits at location 1FA9H.

P1_PIN (1FA9H)

7	6	5	4	3	2	1	0
PIN7*	PIN6*	PIN5*	PIN4	PIN3	PIN2	PIN1	PIN0

* = THIS BIT RESERVED ON 8XC196MC.

Figure 3.1. P1_PIN Register

CHAPTER 4
PORT 7

Port 7 is an 8-bit bi-directional CMOS level port featuring schmitt trigger inputs.

Port configuration and operation is the same as I/O port 2, so refer to Chapter 5 in the 8XC196MC User's Manual for information on this. Port 7 SFR's are listed here for reference:

Table 4.1. Port 7 SFR's

SFR	Address	Reset Value
P7_PIN	1FD7H	xxH
P7_REG	1FD5H	0FFH
P7_DIR	1FD3H	0FFH
P7_MODE	1FD1H	00H

Several of the port 7 pins have special functions assigned to them. These are listed in Table 4.2.

Table 4.2. Port 7 Special Functions

PIN	PRIMARY FUNCTION	SPECIAL FUNCTION
P7.0	I/O	CAPCOMP4
P7.1	I/O	CAPCOMP5
P7.2	I/O	COMPARE4
P7.3	I/O	COMPARE5
P7.4	I/O	—
P7.5	I/O	—
P7.6	I/O	—
P7.7	I/O	FREQOUT

The special function is selected by writing a 1 to the corresponding bit in P7_MODE.

Pins P7.0-3 are assigned to the additional EPA channels, while P7.7 is assigned to the Frequency Generator output.

New EPA Channels 5

CHAPTER 5
NEW EPA CHANNELS

Two new capture/compare and two compare only modules have been added to the EPA structure. The SFR locations for these registers is detailed in Table 5.1.

Figure 5.1. New EPA Channels

Module Name	SFR Address
COMP5_TIME	1F6EH (Word)
COMP5_CON	1F6CH (Byte)
COMP4_TIME	1F6AH (Word)
COMP4_CON	1F68H (Byte)
CAPCOMP5_TIME	1F56H (Word)
CAPCOMP5_CON	1F54H (Byte)
CAPCOMP4_TIME	1F52H (Word)
CAPCOMP4_CON	1F50H (Byte)

Programming of these new EPA channels is identical to the existing 8XC196MC channels, and is described in Chapter 6 of the *8XC196MC USER'S MANUAL.*

Note that all _TIME registers must be written as words.

New Interrupts 6

CHAPTER 6
NEW INTERRUPTS

The additional 4 EPA channels described in Section 5 have new interrupt control bits and vectors assigned to them. Figure 6.1 details the new interrupt pending bits.

INT_PEND (0009H)

7	6	5	4	3	2	1	0
COMP2	CAPCOM2	COMP1	CAPCOM1	COMP0	CAPCOM0	AD_DONE	TOVF

INT_PEND1 (0012H)

7	6	5	4	3	2	1	0
RSV	EXTINT	PI	CAPCOM5*	COMP4*	CAPCOM4*	COMP3	CAPCOM3

RSV = RESERVED BIT. MUST WRITE AS 0

*** = NEW BIT ON 8XC196MD. MUST WRITE AS 0 IF USING 8XC196MC**

Figure 6.1. 8XC196MD Interrupt Pending Registers

The PI interrupt bit is a "shared" interrupt, and multiplex the WG and COMP5 interrupts together. This is illustrated in Figure 6.2.

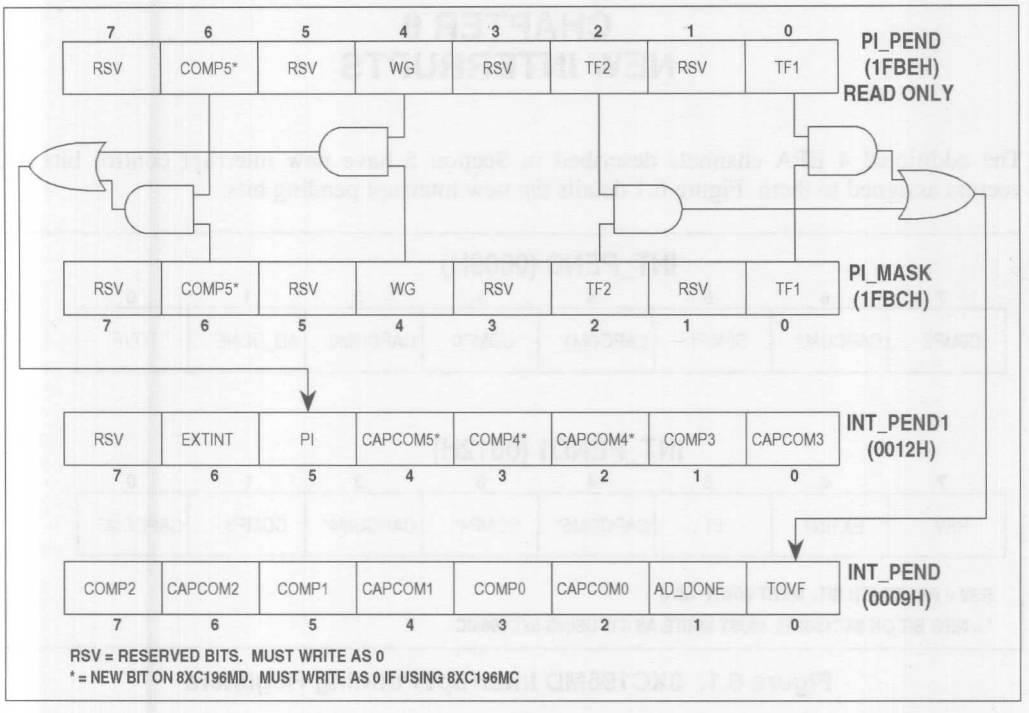

Figure 6.2. 8XC196MD interrupt sharing

Note that the COMP5 module interrupt pending bit is shared with the WG interrupt, and generates the PI interrupt vector.

The INTMASK1 register has additional bits to control the CAPCOM5, COMP4, and CAPCOM4 interrupts. These are detailed in Figure 6.3

INT_MASK (0008H)

7	6	5	4	3	2	1	0
COMP2	CAPCOM2	COMP1	CAPCOM1	COMP0	CAPCOM0	AD_DONE	TOVF

INT_MASK1 (0013H)

7	6	5	4	3	2	1	0
RSV	EXTINT	PI	CAPCOM5*	COMP4*	CAPCOM4*	COMP3	CAPCOM3

RSV = RESERVED BIT. MUST WRITE AS 0

* = NEW BIT ON 8XC196MD. MUST WRITE AS 0 IF USING 8XC196MC

Figure 6.3. 8XC196MD Interrupt Mask Registers

Additionally, the new interrupts can generate PTS cycles. There are new bits in the PTSSEL and PTSSRV registers that support this, as shown in Figure 6.4.

PSSSEL (0004H) and PTSSRV (0006H)

15	14	13	12	11	10	9	8
RSV	EXTINT	PI	CAPCOM5*	COMP4*	CAPCOM4*	COMP3	CAPCOM3

7	6	5	4	3	2	1	0
COMP2	CAPCOM2	COMP1	CAPCOM1	COMP0	CAPCOM0	AD_DONE	TOVF

RSV = RESERVED BIT. MUST WRITE AS 0

* = NEW BIT ON 8XC196MD. MUST WRITE AS 0 IF USING 8XC196MC

Figure 6.4. 8XC196MD PTSSEL and PTSSRV Registers

Note that the bit names and positions are the same for both the PTSSEL and PTSSRV registers.

The new interrupts have new vector table locations assigned to them. Table 6.1 lists the source, priority, and location of all the interrupt vectors on the 8XC196MD device.

Table 6.1. 8XC196MD Interrupt Sources, Vectors, and Priorities

Interrupt Source	Symbol	Interrupt Service			PTS Service		
		Name	Vector	Priority	Name	Vector	Priority
NMI	NMI	INT15	0203EH	30	—	—	—
EXTINT Pin	EXTINT	INT14	0203CH	14	PTS14	0205CH	29
Peripheral Interrupt*	PI	INT13	0203AH	13	PTS13*	0205AH	28
Capture/Compare5**	CAPCOM5	INT12	02038H	12	PTS12	02058H	27
Compare4**	COMP4	INT11	02036H	11	PTS11	02056H	26
Capture/Cmpare4**	CAPCOM4	INT10	02034H	10	PTS10	02054H	25
Compare3	COMP3	INT09	02032H	09	PTS09	02052H	24
Capture/Compare3	CAPCOM3	INT08	02030H	08	PTS08	02050H	23
Unimplemented Opcode	—	—	02012H	—	—	—	—
Software TRAP Instruction	—	—	02010H	—	—	—	—
Compare2	COMP2	INT07	0200EH	07	PTS07	0204EH	22
Capture/Compare2	CAPCOM2	INT06	0200CH	06	PTS06	0204CH	21
Compare1	COMP1	INT05	0200AH	05	PTS05	0204AH	20
Capture/Compare1	CAPCOM1	INT04	02008H	04	PTS04	02048H	19
Compare0	COMP0	INT03	02006H	03	PTS03	02046H	18
Capture/Compare0	CAPCOM0	INT02	02004H	02	PTS02	02044H	17
A/D Conversion Complete	AD_DONE	INT01	02002H	01	PTS01	02042H	16
Timer Overflow*	TOVF	INT00	02000H	00	PTS00*	02040H	15

* This is a shared interrupt from the PI_PEND register. Be aware that the PTS cannot determine the source of the PI or TOVF interrupt.

** These interrupts only exist on the 8XC196MD. They are reserved on the 8XC196MC.

The Frequency Generator 7

CHAPTER 7
THE FREQUENCY GENERATOR

The Frequency Generator (FG) peripheral produces a fixed 50% duty cycle waveform that can vary in frequency from 4 KHz to 1 MHz (@ XTAL1 = 16 MHz). There are 2 Special Function Registers (SFR's) directly associated with the Frequency Generator, FREQ_GEN and FREQ_CNT. Additionally, P7.7 must be configured for its special function in order for the frequency to be output. Figure 7.1 shows a block diagram of the FG.

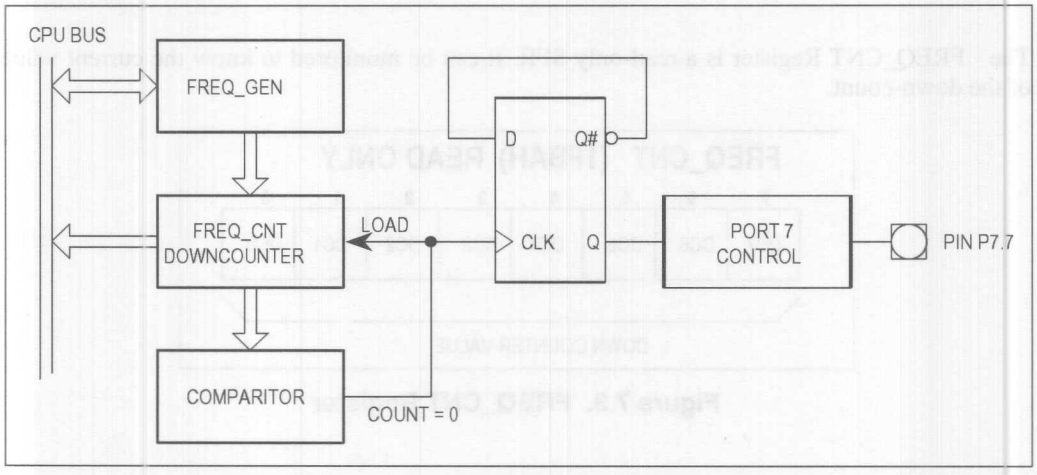

Figure 7.1. The Frequency Generator

When a value is written to FREQ_GEN, it is transferred to the down counter. The down counter repitively counts down to 0 and reloads from FREQ_GEN. Each reload toggles the D flip-flop, thus producing the 50% duty cycle output.

Figures 7.2 and 7.3 detail the FREQ_GEN and FREQ_CNT SFR's. FREQ_GEN is an 8-bit read/write register which controls the frequency of the FG. To calculate the value to load into FREQ_GEN, use the following formula:

$$\text{FREQ\_GEN\_VALUE} = \frac{\text{Fxtal1}}{16 \times \text{FREQ\_OUT}} - 1$$

where

FREQ_GEN_VALUE = 8-bit value to load into FREQ_GEN
Fxtal = Frequency input on XTAL1 pin, MHz
FREQ_OUT = Output frequency, MHz

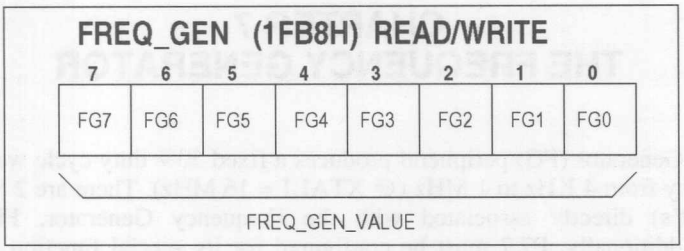

Figure 7.2. FREQ_GEN Register

The FREQ_CNT Register is a read-only SFR. It can be monitored to know the current value of the down-count.

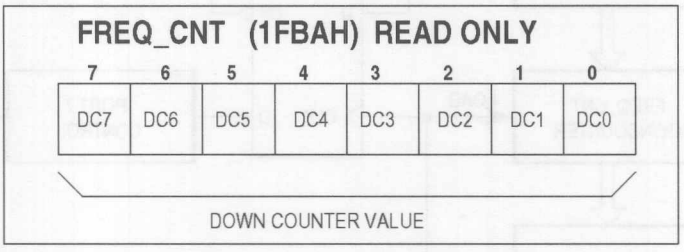

Figure 7.3. FREQ_CNT Register

7.1 USING THE FREQUENCY GENERATOR

One application for the FG is to drive an infrared (IR) LED to transmit remote control data and/or control signals. Figure 7.4 illustrates how the IR remote control system works.

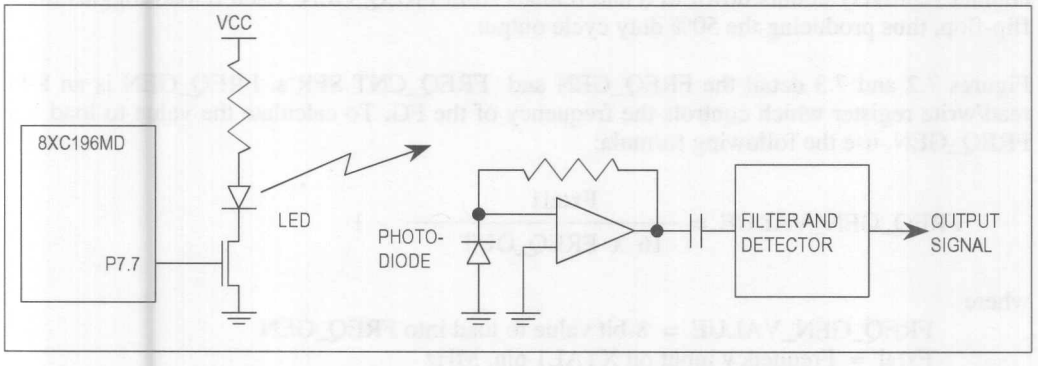

Figure 7.4. Infrared Remote Control Block Diagram

The FG is set to a carrier frequency in the 40 KHz range, and is switched on and off by writing to the P7.7_MODE register. Information is transmitted in a serial format; many coding schemes are possible, Figure 7.5 illustrates one possible code sequence that can be used.

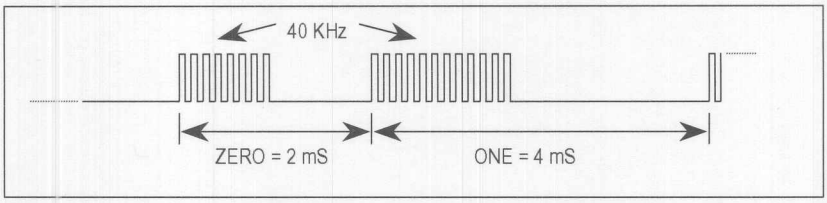

Figure 7.5. Encoding of Zeros and Ones

Zeros are represented by a 1mS carrier burst followed by a 1 mS pause. One's are represented by a 2 mS carrier burst followed by a 2 mS pause.

At the receiving end, a photodiode receives the light pulses. Since there is a great deal of ambient light, a high-pass filter rejects the low-frequency background light, while allowing the 40 KHz carrier to pass. This carrier is amplified and detected to reproduce the original pulse sequence.

SECTION II

Errata for 8XC196MC User's Manual, #272181-001

ERRATA FOR 8XC196MC USER'S MANUAL, #272181-001

Page 1-1, figure 1.1 8XC196MC Block Diagram

The block diagram is not very accurate. Use this new block diagram:

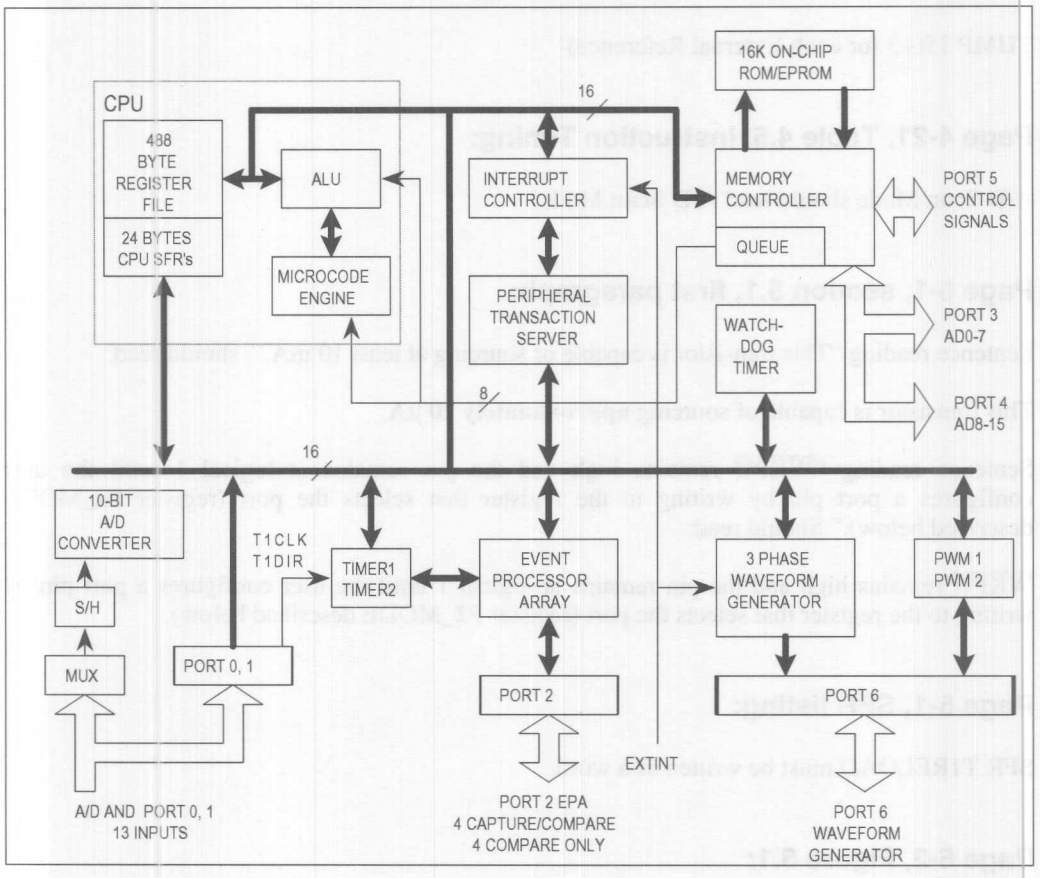

Figure 1.1. 8XC196MC Block Diagram

Page 2-1, second paragraph:

Sentence reading "In addition, an 8-bit CPU bus transfers instruction bytes from the memory device to the instruction register in the RALU."

should read: In addition, an 8-bit instruction bus transfers instruction bytes from the prefetch queue to the instruction register in the RALU.

Page 4-19, Table 4.5. Instruction Timing:

MULUB (3 op) indirect auto increment mode is **13/15** state times.

STB indirect auto increment mode is 6/**8** state times.

Page 4-20, Table 4.5. Instruction Timing:

TIJMP 15(+3 for **each** External Reference)

Page 4-21, Table 4.5. Instruction Timing:

A/D Soan Mode should read A/D **Scan** Mode.

Page 5-1, section 5.1, first paragraph:

Sentence reading "This transistor is capable of sourcing at least 10 mA." should read:

This transistor is capable of sourcing **approximately 10 μA**.

Sentence reading "$\overline{\text{WKPU}}$ remains high and the pin remains at logical 1 until the user configures a port pin by writing to the register that selects the port (register Pz_MODE described below)." Should read:

$\overline{\text{WKPU}}$ remains high and the pin remains at logical 1 until the user configures a port pin by writing to the register that selects the port (register P**2**_MODE described below).

Page 6-1, SFR listing:

SFR T1RELOAD must be written as a word.

Page 6-2, Figure 6.1:

Figure 6.1 EPA Timer/Counters is incorrect. The corrected drawing is given here:

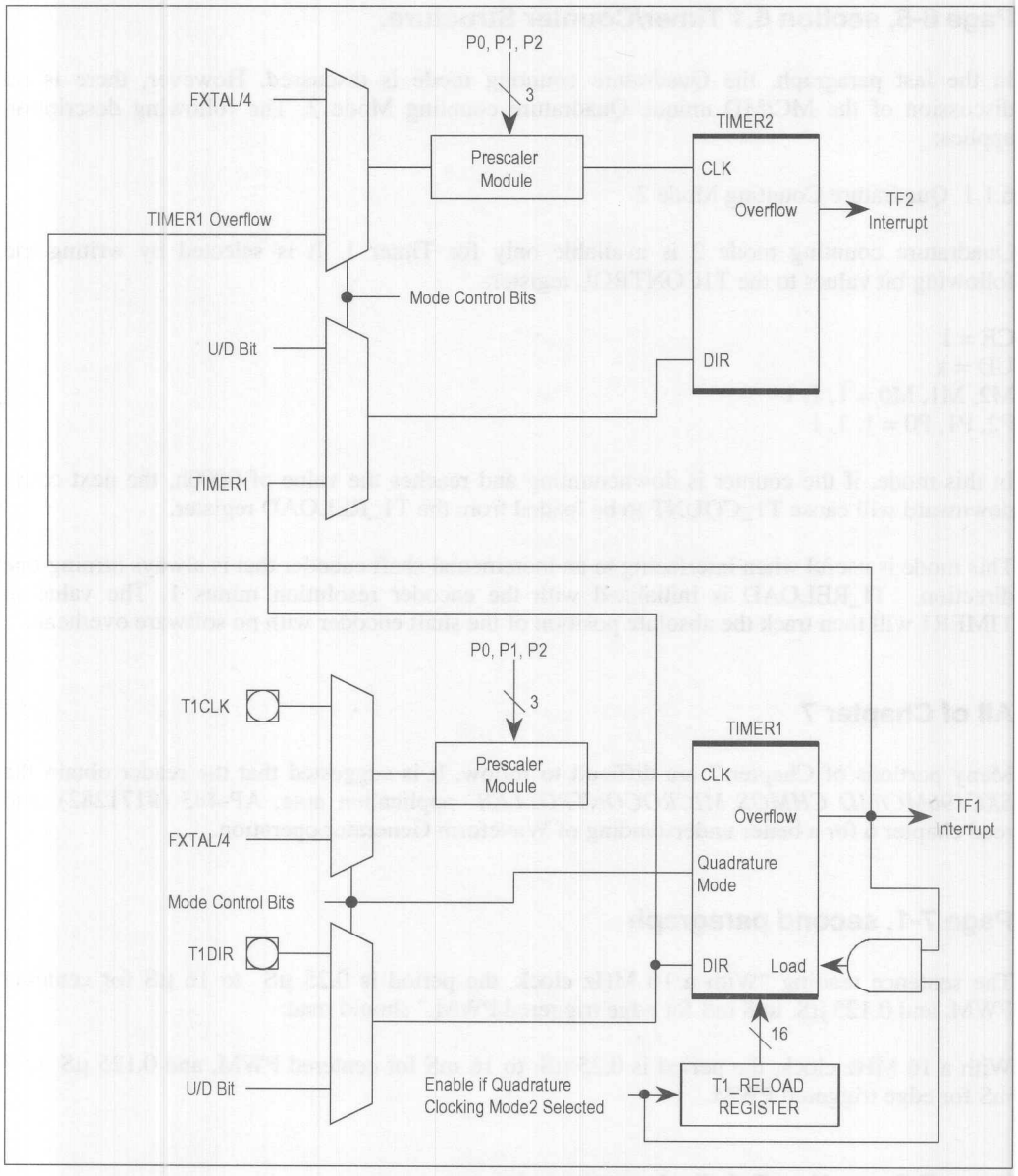

Figure 6.1. EPA Timer/Counters

Page 6-5, section 6.1 Timer/Counter Structure.

In the last paragraph, the Quadrature counting mode is discussed. However, there is no discussion of the MC/MD unique Quadrature counting Mode 2. The following description applies:

6.1.1 Quadrature Counting Mode 2

Quadrature counting mode 2 is available only for Timer 1. It is selected by writing the following bit values to the T1CONTROL register:

CE = 1
UD = x
M2, M1, M0 = 1, 1, 1
P2, P1, P0 = 1, 1, 1

In this mode, if the counter is downcounting and reaches the value of 0000h, the next count downward will cause T1_COUNT to be loaded from the T1_RELOAD register.

This mode is useful when interfacing to an incremental shaft encoder that is always turning one direction. TI_RELOAD is initialized with the encoder resolution minus 1. The value in TIMER1 will then track the absolute position of the shaft encoder with no software overhead.

All of Chapter 7

Many portions of Chapter 7 are difficult to follow. It is suggested that the reader obtain the *8XC196MC/MD CHMOS MICROCONTROLLER* application note, AP-483 (#171282), and read chapter 6 for a better understanding of Waveform Generator operation.

Page 7-1, second paragraph

The sentence reading "With a 16 MHz clock, the period is 0.25 µS to 16 µS for centered PWM, and 0.125 µS to 8 mS for edge triggered PWM." should read:

With a 16 MHz clock, the period is 0.25 µS to 16 **mS** for centered PWM, and 0.125 µS to 8 mS for edge triggered PWM.

Page 7-3, section 7.4, first paragraph

The last sentence reads "The response time may be as fast as two states or if noise immunity is desired, a digital filter can scan the input signal for 16 states to pass any noise." should read:

The minimum response time is **3** state times, selected by the edge mode (ES = 0). If greater noise immunity is desired, select the level mode (ES = 1). In level mode, the input is sampled 3 times over a **24** state-time interval. If all three samples are valid, the EXTNT event will be recognized.

Page 8-2, section 8.1

The formula for PWM frequency has an error. The correct formula is shown below:

$$FREQ = \frac{Fxtal}{512 \times (PWM\_PERIOD\_VALUE + 1)}$$

where

Fxtal = processor clock frequency on XTAL1 pin, Hz
FREQ = output frequency of PWM, Hz
PWM_PERIOD_VALUE = 8-bit value loaded into PWM_PERIOD

Page 9-3, section 9.1.1

The last sentence is cut off. The complete sentence should read:

If this happens, the conversion in progress is aborted and the new one is started. The TD bit selects the A/D operation as a Normal Conversion (TD=0) or a Threshold Detect (TD=1).

Page 9-10, first paragraph

The last sentence which reads "VREF and VCC should power-up at the same time to prevent a possible catch-up condition occurring on VREF." is in error.

It is **not necessary** to power VREF and VCC at the same time to prevent **latch-up**. However, negative voltage spikes on the ANGND pin can cause the A/D converter circuitry to latch up. For this reason, is advised that ANGND be connected to Vss at a SINGLE location as close to the device as possible. Also, it is recommended that a 1 µF ceramic or tantalum capacitor be connected from VREF to ANGND as close to the device as possible. This is because during conversions, current pulses are drawn by the internal VREF circuitry. This capacitor is necessary to keep the reference voltage constant during conversions.

Page 9-10, second paragraph

The last sentence reads "If the difference between ANGD and Vss exceeds 0.4V, the device may catch-up." should read:

If the difference between **ANGND** and Vss exceeds **0.5V**, the device may **latch-up**.

Chapter 11\12 Interrupts/PTS

There is more detailed information on interrupts and the PTS in the 8XC196MC/MD CHMOS MICROCONTROLLER application note, AP-483 (#272282). The user should read chapter 1 for additional information.

Page 11-3 table 11.1

The vector location for INT07 (COMPARE2) is incorrect. The correct vector location is 200EH.

Page 11-4, section 11.1.1

The manual left out the following information:

The PI_PEND register is a read only SFR. PI_PEND is cleared when read, so if more than one bit needs to be checked the register must be preserved in a "shadow" register. Writes to this register will have no effect.

Also note that the PI_PEND register multiplexes the TF1 and TF2 interrupts to the TOVF pending bit in INT_PEND, and the WG interrupt causes the PI pending bit to be set in INT_PEND1. The following figure clarifies this:

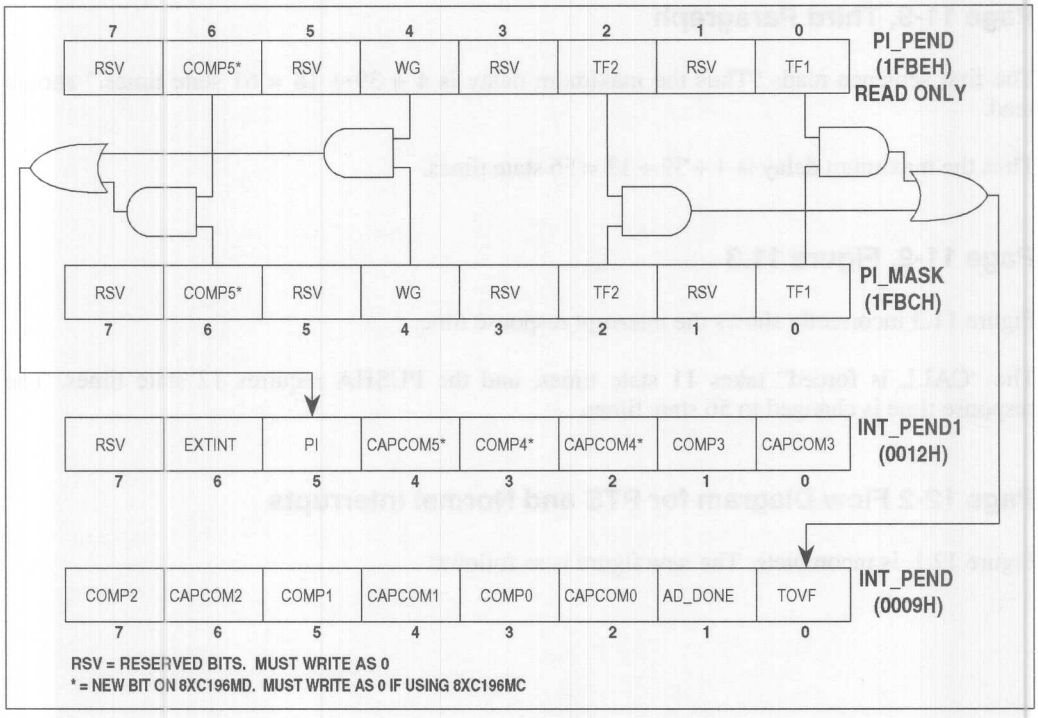

Figure 11.x. Interrupt Sharing

Page 11-8, Section 11.4

The first sentence reads "There are six instructions that always inhibit interrupt acknowledgment until after the following instruction has been executed: DI, EI, PUSHF, POPF, PUSHA, POPA." Should read:

There are eight instructions that always inhibit interrupt acknowledgment until after the following instruction has been executed: DI, **DPTS**, EI, **EPTS**, PUSHF, POPF, PUSHA, POPA.

Page 11-9, Second Paragraph

Item 3. in the list reads "The response time (16 state times for an internal stack or 18 for an external stack)." should read:

The response time (**11** state times for an internal stack or **13** for an external stack).

Page 11-9, Third Paragraph

The first sentence reads "Thus the maximum delay is 4 + 39 + 18 = 61 state times." should read:

Thus the maximum delay is 4 + 39 + 13 = 56 state times.

Page 11-9, Figure 11.3

Figure 11.3 incorrectly shows the interrupt response time.

The "CALL is forced" takes 11 state times, and the PUSHA requires 12 state times. The response time is changed to 56 state times.

Page 12-2 Flow Diagram for PTS and Normal Interrupts

Figure 12.1. is incomplete. The new figure is as follows:

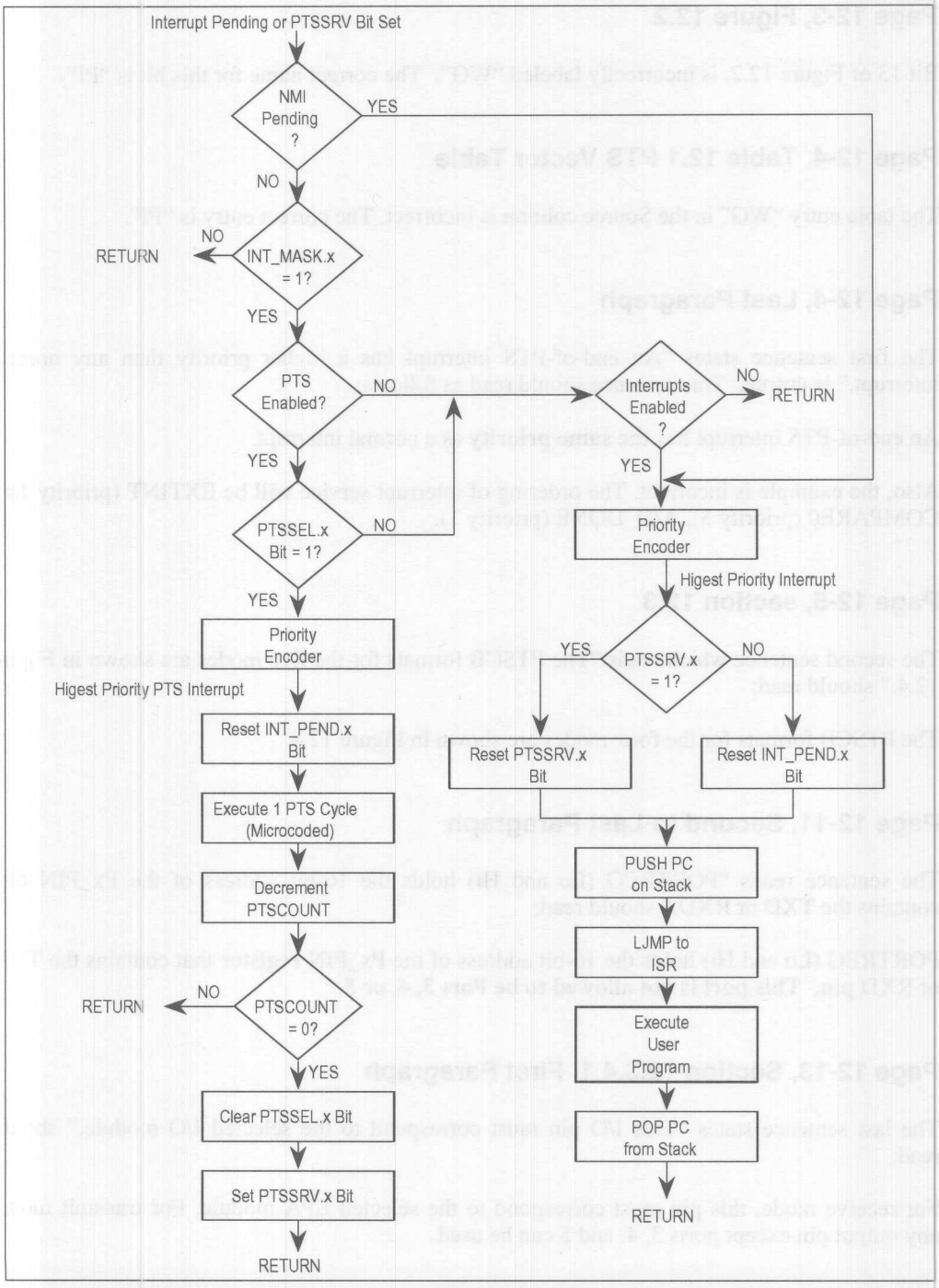

Figure 12.1. Flow Diagram for PTS and Normal Interrupts

Page 12-3, Figure 12.2

Bit 13 of Figure 12.2. is incorrectly labeled "WG". The correct name for this bit is "PI".

Page 12-4, Table 12.1 PTS Vector Table

The table entry "WG" in the Source column is incorrect. The correct entry is "PI".

Page 12-4, Last Paragraph

The first sentence states "An end-of-PTS interrupt has a higher priority than any normal interrupt." is untrue. This sentence should read as follows:

An end-of-PTS interrupt has **the same priority** as a normal interrupt.

Also, the example is incorrect. The ordering of interrupt service will be EXTINT (priority 14), COMPARE0 (priority 3), A/D_DONE (priority 1).

Page 12-5, section 12.3

The second sentence which reads "The PTSCB formats for the five modes are shown in Figure 12.4." should read:

The PTSCB formats for the **four** modes are shown in Figure 12.4.

Page 12-11, Second to Last Paragraph

The sentence reads "PORTREG (Lo and Hi) holds the 16-bit address of the Px_PIN that contains the TXD or RXD." should read:

PORTREG (Lo and Hi) holds the 16-bit address of the Px_PIN **register** that contains the TXD or RXD **pin**. **This port is not allowed to be Port 3, 4, or 5.**

Page 12-13, Section 12.3.4.1, First Paragraph

The last sentence states "This I/O pin must correspond to the selected I/O module." should read:

For receive mode, this pin must correspond to the selected EPA module. For transmit mode, any output pin except ports 3, 4, and 5 can be used.

Page 12-17, Paragraph Labeled 1.

The line which reads "--P2_MODE = 1 (select port function)" is incorrect. it should read as follows:

--P2_MODE = 0 (select port function)

Page 12-19 Figure 12.17.

This figure is incorrectly titled "Asynchronous Baud Rate Equation". The correct title is:

Synchronous Baud Rate Equation

Page 12-19, Section 12.3.4.5, First paragraph

The third sentence incorrectly states "Any SFR I/O pin may be used for data." The correct sentence is:

Any SFR I/O pin **except for ports 3, 4, and 5** may be used for data.

Page 12-21, Section 12.3.4.6, First paragraph

The fifth sentence incorrectly states "Any SFR I/O pin may be used for data." The correct sentence is:

Any SFR **output** pin **except for ports 3, 4, and 5** may be used for data.

Pages 16-1 and 16-2 Section 16.1

The power-up and power-down sequencing for programming is a bit confusing. A new sequence has been defined as follows:

POWER-UP SEQUENCE

1. When first powering up, the device must be held in reset while V_{CC} stabilizes. V_{PP} and $\overline{EA}$ must be allowed to float during this time.
2. Continue holding the device in reset after V_{CC} has stabilized, and apply +12.50 volts to $\overline{EA}$ and V_{PP}. Refer to the data sheet for exact specifications on this voltage. **NOTE: Applying voltage to V_{PP} when V_{CC} is low will permanently damage the device.**
3. Allow time for $\overline{EA}$ and V_{PP} to be within tolerance, and for the oscillator to stabilize.
4. After condition 3 is met, $\overline{RESET}$ may be allowed to rise.

5. After completion of the programming sequence the power-down sequence should followed.

POWER-DOWN SEQUENCE

1. Assert the $\overline{\text{RESET}}$ signal ($\overline{\text{RESET}}$ = 0). RESET must be held low throughout the powerdown sequence. Do not allow the reset signal to "bounce" or another programming sequence will begin.
2. Remove the +12.5 volts applied to $\overline{\text{EA}}$ and V_{PP} and allow these pins to float. **$\overline{\text{EA}}$ and V_{PP} must be allowed to float before removing V_{CC} or the device will be damaged.**
3. Turn off the V_{CC} supply and allow time for this to reach 0 volts.
4. The device may now be removed from the programming circuit.

Appendix B, Page B-47

The PUSHF instruction operation is incorrectly detailed. The correct information is as follows:

SP <-------- SP - 2
(SP) <------- PSW **and INT_MASK**
PSW <------- 0
INT_MASK <--- 0